

HYBRID SUBSTRATE AND METHOD FOR FABRICATING THE SAME**Field of the Invention**

This invention relates to the field of integrated circuit (IC) design. Specifically, it relates to a hybrid substrate and method for fabricating the same.

BACKGROUND OF THE INVENTION

Wafer bonding (also called wafer fusion) techniques have been extensively practiced for different applications requiring different substrates. These techniques enable two different wafers to be bonded together, so that fabrication of highly lattice-mismatched and orientation-mismatched heterostructures become possible without generating threading dislocations. For example, wafer bonding techniques have been utilized to form silicon-on-oxide (SOI) substrate, and for bonding III-V materials with other materials.

The prior art wafer bonding techniques, however, do not provide for fabricating a hybrid substrate by integrating three or more different types of material on a common carrier substrate. It is desirable to have a system chip which includes mixed devices, such as laser diodes for external communication, rf or microwave high-power, high-frequency devices for transmitting and receiving data, and high density, low-power silicon devices for logic and memory.

As an example, GaN-based high-electron mobility transistors (HEMTs) are known to have high saturation velocity and enhanced mobility in nitride semiconductor heterostructures. Accordingly, they are suitable for high-power applications at microwave frequencies. These devices are typically built on a GaN on sapphire substrate or a SiC substrate.

On the other hand, optoelectronic devices are typically built on a substrate formed by III-V materials. For example, InGaAsP/InP edge-emitting lasers are usually fabricated using InP over a silicon substrate. The bonding process entails first depositing a p-type InP substrate and capping it with a p-type InGaAs film. Second, a n-type InP substrate is deposited over the film. The n-type InP substrate is then bonded to the silicon substrate. The bonded wafer is then annealed at 400 degrees Celsius.

In order to create a sophisticated system, for example, a system having GaN based high-electron mobility-transistors and optoelectronic devices to realize more applications, it is required to integrate such different devices on more than two different substrates. It is therefore required to provide a substrate having multiple materials, i.e., a hybrid substrate, where each material can be used for fabricating one or more different devices. For example, one material can be used for fabricating the GaN based high-electron mobility-transistors, another material can be used for fabricating the optoelectronic devices, and another material can be used for high-density, low-power Si-based devices..

Additionally, by providing a hybrid substrate, chips fabricated from different materials can be fabricated on the hybrid substrate. For example, a first part of the hybrid substrate can be used for fabricating a GaAs chip, a second part of the hybrid substrate can be used for fabricating an InP chip, and a third part of the hybrid substrate can be used for fabricating a silicon chip.

SUMMARY

An aspect of the present invention is to provide a hybrid substrate, i.e., a substrate fabricated from different materials, and method for fabricating the same.

Another aspect of the present invention is to provide a hybrid substrate configured for fabricating more than two different devices thereon.

Further, another aspect of the present invention is to provide a hybrid substrate having a high thermal conductivity.

Finally, another aspect of the present invention is to provide a hybrid substrate configured for patterning interconnects thereon for interconnecting different devices fabricated on the hybrid substrate. This would greatly reduce the size of a system fabricated on the hybrid substrate, since the patterned interconnects would eliminate contact pads, and wide metal wirings used in prior art systems. Further, inductive noise caused by the wide metal wirings would also be reduced.

These aspects are realized by the present invention which provides a hybrid substrate. The hybrid substrate is configured for fabricating more than two different devices thereon, has a high thermal conductivity, and is configured for patterning interconnects thereon for interconnecting the different devices fabricated on the hybrid substrate. The hybrid substrate

includes a substrate having a plurality of pockets patterned thereon; and at least two different materials provided within a respective pocket of the plurality of pockets. The at least two different materials are planarized, such that a top surface of the at least two different materials is approximately co-planar with a top surface of the substrate. Further, the at least two different materials are bonded to the substrate.

Further, the present invention presents a method for fabricating the hybrid substrate. The method includes the steps of patterning a substrate with a plurality of pockets; and providing a material within each of the plurality of pockets, wherein at least two materials provided within two respective pockets of the plurality of pockets are different. The method further includes the step of planarizing the materials provided within each of the plurality of pockets, such that a top surface of the materials is approximately co-planar with a top surface of the substrate. Further still, the method includes the step of providing a thermal conductivity layer between the substrate and the material provided within each of the plurality of pockets.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a cross-sectional view of a portion of a carrier substrate for fabricating the hybrid substrate according to the present invention; and

FIGS. 2-6 are cross-sectional views illustrating a preferred process for fabricating the hybrid substrate according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a hybrid substrate, i.e., a substrate fabricated from different materials, and method for fabricating the same. The hybrid substrate is configured for fabricating more than two different devices thereon, has a high thermal conductivity, and is configured for patterning interconnects thereon for interconnecting the different devices fabricated on the hybrid substrate.

FIG. 1 is a cross-sectional view of a portion of a carrier substrate 100 for fabricating the hybrid substrate according to the present invention. The carrier substrate 100 is preferably fabricated from aluminum nitride (AlN). AlN is a desirable substrate for the carrier substrate 100 due to its ability to support a wide variety of materials provided thereon

due to its high thermal conductivity. Other preferred materials for the carrier substrate 100 include quartz, glass, ceramic, CVD diamond, and sapphire.

A description of the preferred method for fabricating the hybrid substrate will now be provided. With reference to FIGS. 2-6 there are shown cross-sectional views of the preferred method for fabricating the hybrid substrate.

With reference to FIG. 2, the carrier substrate 100 is patterned and etched to form pockets 120A, 120B, and 120C. The pockets 120A, 120B, and 120C will be used to place different materials therein. The depth of the pockets 120A, 120B, and 120C is in the range of 5um to 50um.

With reference to FIG. 3, a layer of CVD diamond 130 is deposited over the etched carrier substrate. CVD diamond is preferred since it has very good thermal conductivity in dissipating heat generated from the various devices provided over the hybrid substrate. The thickness of the layer of CVD diamond is in the range of 100nm to 1000nm.

With reference to FIG. 4, different materials, such as GaAs, InP, and silicon wafer, 150A, 150B, and 150C, respectively, are provided within the pockets 120A, 120B, and 120C. These materials may have different thicknesses, e.g., t1, t2, and t3, respectively. Preferably, as indicated by reference numeral 160 in FIG. 4, there is a gap between each cut material and the layer of CVD diamond 130, since the cut material size is slightly smaller than the etched pocket dimensions to guarantee that each cut material can fit into its respective pocket. It is contemplated that other materials can be provided within the pockets 120A, 120B, and 120C besides GaAs, InP and silicon wafer, such as GaN-based high-electron mobility transistors (HEMTs) and optoelectronic devices formed by III-V materials, such as InGaAsP/InP edge-emitting lasers fabricated using InP over a silicon substrate.

Further, it is preferable to apply a thin oxide layer on top of each material 150A, 150B, and 150C before dicing. This oxide layer is faced to the deposited diamond CVD layer 130 to enhance bonding strength between the different materials 150A, 150B, and 150C and the carrier substrate 100, after preferably applying an annealing step to adhere the materials 150A, 150B, and 150C to the carrier substrate 100.

Prior to dicing the materials 150A, 150B, and 150C, the materials 150A, 150B, and 150C can be prepared using the blister separation method as known in the art, e.g., the blister separation method described in U.S. Patent No. 6,159,824, in order that a major portion of

the materials 150A, 150B, and 150C can easily be removed before planarizing the materials 150A, 150B, and 150C as further described below with reference to FIG. 6. The removed portions of each material 150A, 150B, and 150C can possibly be used again in manufacturing another system chip device to save on material costs.

5 With reference to FIG. 5, a layer of CVD oxide 180 is deposited to cover the surface. After the layer of CVD oxide 180 is deposited, a final annealing process is performed. The layer of CVD oxide 180 fills in the gaps between the materials 150A, 150B, and 150C and the pockets 120A, 120B, and 120C.

10 With reference to FIG. 6, a chem-mech polish step is performed to planarize the materials 150A, 150B, and 150C to the diamond film surface 130. After the chem-mech polish step, all the materials 150A, 150B, and 150C are approximately co-planar with the diamond film surface 130.

15 The finished hybrid substrate designated by reference numeral 190 in FIG. 6 is ready for fabricating different devices thereon. Preferably, common interconnect structures can be provided to interconnect the different materials 150A, 150B, and 150C and to provide for communications between the different materials 150A, 150B, and 150C.

20 The advantages of the hybrid substrate 190 of the present invention are the following: (1) no alignment is required when merging the prefabricated chips together on one carrier substrate, as opposed to performing a precision alignment, as in the prior art, when merging prefabricated chips; (2) devices are fabricated on surfaces which are fully planarized, as opposed to fabricating the devices on non-planarized surfaces, as in the prior art, which makes it difficult to interconnect the devices; (3) the process of bonding the materials 150A, 150B, and 150C is less complicated and prone to defects, since there are no devices fabricated on the materials 150A, 150B, and 150C when the materials 150A, 150B, and 150C are bonded to the carrier substrate 100, as is the case with prior art methods where
25 prefabricated chips and/or devices are bonded to the substrate (since in the prior art methods prefabricated chips and/or devices are bonded to the substrate, the bonding process cannot be performed at high temperatures, since at high temperatures the chips and/or devices could be damaged); and (4) the surface of the hybrid substrate is free from seams, since the CVD
30 oxide layer 180 overlays the surface of the hybrid substrate and fills in any gaps within the hybrid substrate. Therefore, the materials 150A, 150B, and 150C cannot be contaminated by

chemical or other contaminants, as is the case with prior art methods where there may be a gap formed between the prefabricated chips and the substrate allowing for contaminants to be entrapped which can affect yield and reliability.

What has been described herein is merely illustrative of the application of the principles of the present invention. Other arrangements and methods, such as using different substrates, may be implemented by those skilled in the art without departing from the scope and spirit of this invention.

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